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10/649,414	08/26/2003	Yuan-Liang Li	884.695US2	5306

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SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. BOX 2938
MINNEAPOLIS, MN 55402

EXAMINER	
WILSON, SCOTT R	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 04/21/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/649,414	LI, YUAN-LIANG	
	Examiner	Art Unit	
	Scott R. Wilson	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *20030826*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 13-15 are rejected under 35 U.S.C. 102(e) as being anticipated by Yoshimura et al.. As to claim 13, Yoshimura et al., Figure 35, viewed rotated 180°, (col. 35 line 54-67 and col. 36, lines 1-7) discloses an apparatus comprising: means for receiving input optical signals from an input waveguide (324a) on a motherboard (320a), with a photodetector package (328) mounted to a lower surface of a substrate (320b) residing above the motherboard, means for converting the input optical signals to input electrical signals (328); means for processing the input electrical signals with a first IC chip (352) mounted to the substrate, thereby forming output electrical signals; means for converting the output electrical signals to output optical signals via a light-emitting package (326) mounted to the lower surface of the substrate and coupled to an output waveguide, also (324a), to carry the output optical signals; and means for providing power to the first IC chip, the light-emitting package, and the photodetector package through the motherboard, embodied as traces (330) and vias(333) and arranged between the motherboard and the substrate.

As to claim 14, Yoshimura et al, Figure 35, discloses means for generating the input optical signals with a second IC chip (351) mounted to the motherboard, by the combination of substrate (320b) and conductive film (302), and optically coupled to the input waveguide, by the light emitter device (326).

As to claim 15, Yoshimura et al., Figure 37-3, discloses an additional embodiment which includes means for coupling the output optical signals (from (333)) to the output waveguide (324a) and receiving

output optical signals with a third IC chip (3xx) (col. 37, line 28) mounted to the motherboard and optically coupled to the output waveguide.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshimura et al. in view of Tarui. As to claim 1, Yoshimura et al., Figure 35, viewed rotated 180°, (col. 35 line 54-67 and col. 36, lines 1-7) discloses an apparatus used in a method comprising: receiving input optical signals from an input waveguide (324a) on a motherboard (320a), with a photodetector package (328) mounted to a lower surface of a substrate (320b) residing above the motherboard, converting the input optical signals to input electrical signals (328); processing the input electrical signals with a first IC chip (352) mounted to the substrate, thereby forming output electrical signals; converting the output electrical signals to output optical signals via a light-emitting package (326) mounted to the lower surface of the substrate and coupled to an output waveguide, also (324a), to carry the output optical signals; and providing power to the first IC chip, the light-emitting package, and the photodetector package through the motherboard, embodied as traces (330) and vias(333) and arranged between the motherboard and the substrate. Yoshimura et al. does not disclose expressly a capacitive DC shunt coupling motherboard to substrate. Tarui, Figure 5, discloses DC shunt capacitors (2a, 2b, 8a, 8b, 10a and 10b) formed in a high frequency switch. At the time of invention, it would have been obvious to a person of ordinary skill in the art to use DC shunt capacitors to couple motherboard to substrate. The motivation for doing so would have been to isolate the motherboard from the substrate, consistent with applicants background information disclosing the need for decoupling capacitors in order to increase the noise immunity of high-power circuits, such as

CPU's, while still providing for power delivery. Therefore, it would have been obvious to combine Tarui with Yoshimura et al. to obtain the invention as specified in claim 1.

As to claim 2, Yoshimura et al, Figure 35, discloses generating the input optical signals with a second IC chip (351) mounted to the motherboard, by the combination of substrate (320b) and conductive film (302), and optically coupled to the input waveguide, by the light emitter device (326).

As to claim 3, Yoshimura et al., Figure 37-3, discloses an additional embodiment which includes coupling the output optical signals (from (333)) to the output waveguide (324a) and receiving output optical signals with a third IC chip (3xx) (col. 37, line 28) mounted to the motherboard and optically coupled to the output waveguide.

As to claims 4 and 5, Yoshimura et al., col. 38, lines 12-20, discloses an array of light-emitting devices which may be coupled to amplifier-integrated photodetectors.

As to claim 6, Yoshimura et al., col. 38, line 12, discloses a light-emitting VCSEL device. Yoshimura et al., col. 38, lines 15-16, further discloses that a single VCSEL is illustrated for simplicity, and that a plurality of such devices, which is within the scope of an array, are typically used in devices.

As to claim 7, Yoshimura et al, Figure 6 and col. 10, line 42, discloses an alternative embodiment in which a VCSEL may be replaced by a light-emitting diode (LED) array.

As to claim 8, Yoshimura et al, Figure 6 and col. 10, line 42, discloses an alternative embodiment in which a VCSEL may be replaced by a laser diode array.

As to claim 9, Yoshimura et al., Figure 69, and col. 49, line 57, discloses an additional embodiment comprising a microlens array (511) between the light-emitting device (506) and the light-detecting device (508).

Claims 10-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshimura et al. in view of Tarui. As to claim 10, Yoshimura et al., Figure 35, viewed rotated 180°, (col. 35 line 54-67 and col. 36, lines 1-7) discloses a method comprising electrically coupling a first IC chip (351), a light-emitting package (326) and a photodetector package (328) to respective sets of contact-receiving members, embodied as pads, of a substrate, the combination of layers (320b) and (350). Yoshimura et al. does not disclose expressly a capacitive DC shunt coupling a motherboard to the substrate. Tarui, Figure 5,

discloses DC shunt capacitors (2a, 2b, 8a, 8b, 10a and 10b) formed in a high frequency switch. At the time of invention, it would have been obvious to a person of ordinary skill in the art to use DC shunt capacitors to couple motherboard to substrate. The motivation for doing so would have been to isolate the motherboard from the substrate, consistent with applicants background information disclosing the need for decoupling capacitors in order to increase the noise immunity of high-power circuits, such as CPU's, while still providing for power delivery. Therefore, it would have been obvious to combine Tarui with Yoshimura et al. to obtain the invention as specified in claim 10.

As to claim 11, Yoshimura et al., Figure 35, discloses a waveguide, which may be embodied as one or more waveguide arrays (col. 26, lines 6-9), formed in the motherboard (320a).

As to claim 12, Yoshimura et al., Figure 35, discloses receiving input optical signals with the photodetector package (328) from the waveguide array (324a) and generating input electrical signals, which are then transmitted to IC chip (352).

Claims 16-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshimura et al. in view of Tarui. As to claim 16, Yoshimura et al., Figure 35, discloses an apparatus comprising: a motherboard (320a), a substrate (320b) having contact receiving members, akin to (332) of Figure 33 (col. 36, line 8), a first IC chip (352), a light-emitting device (326), which may be a diode (col. 2, line 25), and a photodetector package (328), each electrically coupled to the contact-receiving members. Yoshimura et al. does not disclose expressly a capacitive DC shunt coupling motherboard to substrate. Tarui, Figure 5, discloses DC shunt capacitors (2a, 2b, 8a, 8b, 10a and 10b) formed in a high frequency switch. At the time of invention, it would have been obvious to a person of ordinary skill in the art to use DC shunt capacitors to couple motherboard to substrate. The motivation for doing so would have been to isolate the motherboard from the substrate, consistent with applicants background information disclosing the need for decoupling capacitors in order to increase the noise immunity of high-power circuits, such as CPU's. Therefore, it would have been obvious to combine Tarui with Yoshimura et al. to obtain the invention as specified in claim 16.

As to claim 17, Yoshimura et al., Figure 35, discloses means for aligning, by the placement of contact-receiving members, the light emitting package (326) and photodetector package (328) to the

waveguide (324a), which may be embodied as a waveguide array (col. 26, lines 6-9), formed in the motherboard.

As to claim 18, Yoshimura et al., Figure 35, discloses means for receiving with the photodetector package (328) input optical signals and generating input electrical signals, means for processing the input electrical signals with the first IC ship (352) and generating output electrical signals, and means for receiving the electrical signals with the light-emitting package (326) (via (330) and (351)) and generating output optical signals and outputting the output optical signals.

As to claim 19, Yoshimura et al., col. 38, lines 12-20, discloses an array of light-emitting devices which may be coupled to amplifier-integrated photodetectors.

As to claim 20, Yoshimura et al., col. 38, lines 12-20, discloses the light-emitting array embodied as an array of VCSEL's.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Scott R. Wilson whose telephone number is 703-308-6557. The examiner can normally be reached on M-F 8:30 - 4:30 Eastern.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on 703-308-6601. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-1782.

NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

srw
April 15, 2004